**EXP NO: 13 DATE:**

**MOD-10 COUNTER**

**AIM:**

To write a verilog HDL program for mod-10 counter and verify its output.

**SOFTWARE REQUIRED:**

Xilinx ISE 10.1

**ALGORITHM:**

Step1: Define the specifications and initialize the design.

Step2: Write the source code in VERILOG.

Step3: Check the syntax and perform synthesis .

Step4: Write different combinations of input using the test bench.

Step5:Verify the output by simulating the source code

**VERILOG SOURCE CODE:**

module counter(clk,rst,count);

input clk,rst;

output reg [3:0]count;

always@(posedge clk) begin

if(rst == 1 || count == 9)

count <= 0;

else

count <= count + 1;

end

endmodule

**Test Bench code**

module tb();

reg clk,rst;

wire [3:0]count;

counter c1(clk,rst,count);

initial begin

clk = 0;

forever #5 clk = ~clk;

end

initial begin

rst = 0;

#5 rst = 1;

#10 rst = 0;

#200 $finish;

end

initial

$monitor("%d%d",clk,count);

initial begin

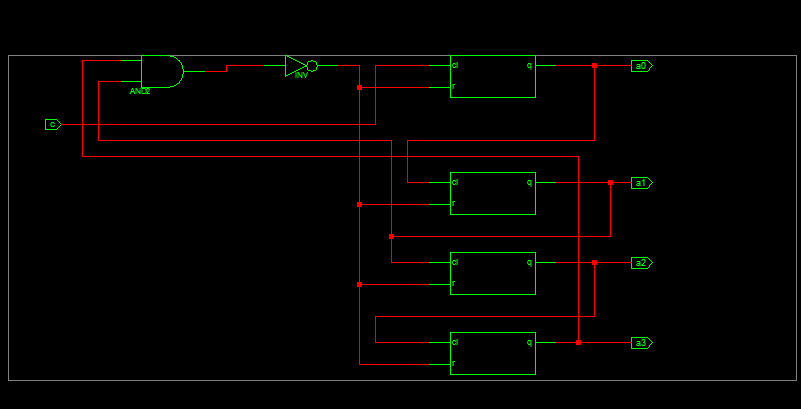
$dumpfile("dump.vcd");

$dumpvars;

end

endmodule

**RTL schematic**



SYNTHESIS REPORT:

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : modten.ngr Top Level Output File Name : modten Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs 6

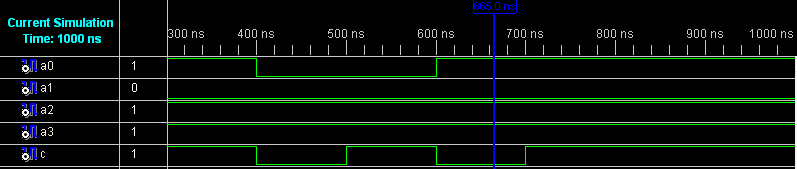
|  |  |
| --- | --- |
| Cell Usage : |  |
| # BELS | : 6 |
| # INV | : 1 |
| # LUT2 | : 1 |
| # LUT2\_L | : 1 |
| # LUT3 | : 1 |
| # LUT4 | : 2 |
| # FlipFlops/Latches | : 4 |
| # FDR | : 4 |
| # Clock Buffers | : 1 |
| # BUFGP | : 1 |
| # IO Buffers | : 5 |
| # IBUF | : 1 |
| # OBUF | : 4 |

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Device utilization summary:

|  |  |  |
| --- | --- | --- |
| Selected Device : | 3s100evq100-4 |  |
| Number of Slices: | 3 out of 960 | 0% |
| Number of Slice Flip Flops: | 4 out of 1920 | 0% |
| Number of 4 input LUTs: | 6 out of 1920 | 0% |
| Number of IOs: | 6 |  |
| Number of bonded IOBs: | 6 out of 66 | 9% |
| Number of GCLKs: | 1 out of 24 | 4% |

SIMULATION OUTPUT:



**RESULT:**

Thus a verilog HDL program was written for mod-10 counter and its output was verified.